HUGHES
SOLID STATE PRODUCTS

CMOS Digital Frequency Synthesizer

HCTR 0320A

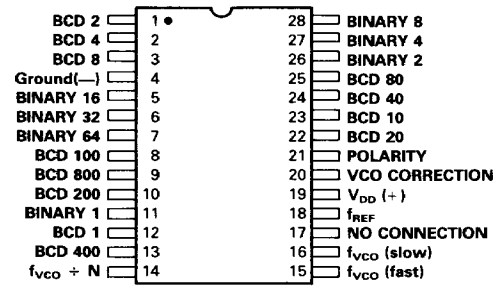
PRELIMINARY DATA

DESCRIPTION

The HCTR 0320 is a CMOS LSI programmable divide by N counter with a phase/frequency detector for frequency synthesis or phase locked loop (PPL) applications. A minimum PPL system can be made using the HCTR 0320, a reference oscillator and divider, low pass filter, and voltage controlled oscillator (VCO). More complex systems may use mixers, frequency multipliers, or a dual modulus prescalar. Most system designs constrain the VCO to oscillate at N times the divided reference oscillator frequency (f_{REF}) so changing N by ΔN changes the VCO frequency by the product (ΔN) • (f_{REF}). Thus multiple VCO frequencies can be generated from only one reference oscillator crystal by varying N. This method results in VCO frequencies which have the same fractional error as the reference crystal oscillator frequency.

FEATURES

- High Frequency Operation (10 MHz)
- Low Power CMOS
- On Chip Phase/Frequency Detector
- BCD and/or Binary Inputs for N
- On Chip Adder to Provide Offset
- N Programmable from 3 to 1023
- VCO Signal Preconditioning
- Output from ÷ N Counter is Provided
- Polarity Control on VCO Correction Signal



ABSOLUTE MAXIMUM RATINGS	SYM.	VALUE	UNIT
DC Supply Voltage	V_{DD}	+15 to −0.3	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain Per Pin, All Inputs*	I	10	mAdc
DC Current Drain Per Pin, All Outputs*	I	20	mAdc
Operating Temperature Range	T_A	−40 to 85°C	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	Pd	600 (plastic pkg) 700 (ceramic pkg)	mW

*Protection diodes forward biased

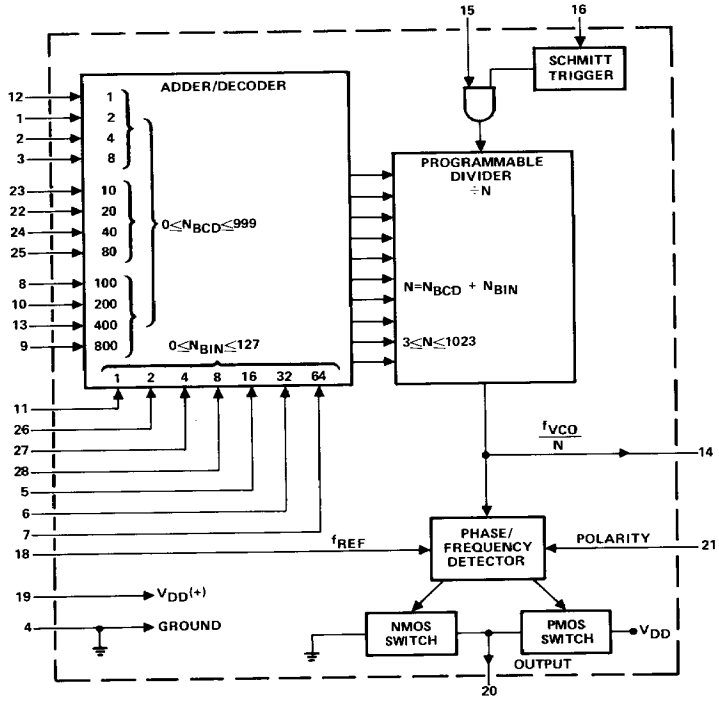
EXPLANATION OF BLOCK DIAGRAM

Adder/Decoder — This block adds a three digit BCD number (N_{BCD}) to a 7 bit binary number (N_{BIN}) to provide a sum equal to the division integer (N). Each decade of BCD inputs is restricted to valid BCD numbers, zero through nine. Positive logic is used.

Programmable Divider — This circuit utilizes a continuously recycling presettable down counter to output a waveform of frequency f_{VCO}/N at a duty cycle of 1/N. f_{VCO} (fast) is the only TTL compatible input and should be used when fast rise and fall times are available and/or maximum speed is required. For input signals with slow rise and fall times such as sine waves, the f_{VCO} (slow) input provides signal preconditioning through a Schmitt Trigger in order to obtain proper rising and falling edges for the digital circuitry. However, the additional circuitry does restrict the maximum operating frequency. The unused f_{VCO} input must be connected to V_{DD} (+). Either f_{VCO} input will accept low frequencies. However, in order to obtain high operating frequencies, dynamic circuitry is used and thus the minimum guaranteed f_{VCO} input frequency is 5KHz.

Phase/Frequency Detector— This block compares the divider output (f_{VCO}/N) with an external reference frequency (f_{REF}) and generates a correction signal. When the VCO correction output goes from the floating state (NMOS and PMOS switches-off) to V_{DD} (+) or GND (—), the indication is that the leading edges of the two input signals do not occur simultaneously. The leading edge of one signal triggers the correction pulse and the leading edge of the other signal resets the output to the floating state (Refer to Timing Diagram). Therefore, the width of the correction pulse is proportional to the time difference between the leading edges. As the two signals approach equal frequency and phase, the width of the pulse becomes narrower and narrower and the two signals are in "lock." The Polarity input should be tied to V_{DD} (+) if the VCO correction output voltage should decrease to cause an increase in the VCO frequency.

CMOS DIGITAL FREQUENCY SYNTHESIZER BLOCK DIAGRAM

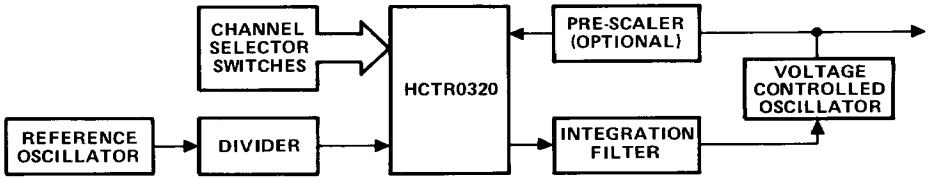


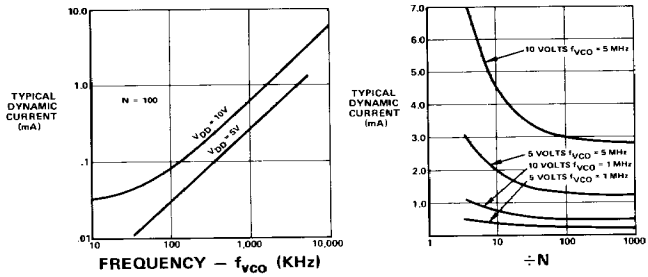
ELECTRICAL SPECIFICATIONS

ELECTRICAL SPECIFICATIONS - Unless otherwise specified T = −40°C to 85°C V_{DD} tolerance = ±5%

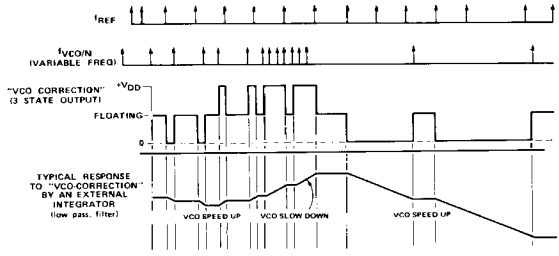
D.C. CHARACTERISTICS		SYMBOL	CONDITIONS		MIN	MAX	UNITS
Supply Voltage		V_{DD}			4.5	13	V
Input Levels							
BCD and Binary Switches	"1"	V_{IH}		5	3.5	5	V
				10	7.0	10	V
	"0"	V_{IL}		5	0	0.8	V
				10	0	1.5	V
f_{VCO} (Fast)	"1"	V_{IH}		5	3.5	5	V
				10	7	10	V
	"0"	V_{IL}		5	0	0.4	V
				10	0	1.0	V
f_{VCO} (Slow), f_{REF}	"1"	V_{IH}		5	4.5	5	V
				10	9	10	V
	"0"	V_{IL}		5	0	0.5	V
				10	0	1.0	V
Input Leakage Current (except BCD and Binary inputs)		I_L	To either V_{DD} or GND	5	–	1	μA
				10	–	2	μA
Input Capacitance		C_L	(Typical)			5	pf
Output Impedance, f_{VCO}/N and VCO Correction		R_{on}	Within 1 Volt of supply	5	–	500	Ω
				10	–	360	
		R_{off}			5	–	M
A.C. CHARACTERISTICS							
Supply Current		I_{DD}	f_{VCO} = 1 MHz N = 100	5	–	0.5	mA
				10	–	1.0	mA
Inputs							
f_{VCO} (Fast)							
Frequency pulse width		F_{VCO}		5	.005	5	MHz
				10	.010	10	MHz
		PW_H	50% to 50%	5	.10	100	μs
		PW_L		10	.045	50	μs
Rise & fall time		t_r, t_f	10% to 90%	5	–	100	ns
				10	–	50	ns
f_{VCO} (Slow)							
Frequency		f_{VCO}		5	.005	2.5	MHz
				10	.010	5	MHz
Pulse width		PW_H,	50% to 50%	5	.200	100	μs
		PW_L		10	.100	50	μs
Rise & fall time		t_r, t_f	10% to 90%	5	No Limit		
				10			
f_{REF} Pulse width		PW_H,	50% to 50%	5	300	–	ns
		PW_L		10	150	–	ns
Rise & fall time		t_r, t_f	10% to 90%	5	–	1	μs
				10	–	1	μs
Outputs							
f_{VCO} (Slow) to f_{VCO}/N propagation delay, falling edge to rising edge		t_{pH}	50% to 50%	5	–	600	ns
			C_L = 10 pf	10	–	250	ns
falling edge to falling edge		t_{pL}	50% to 50%	5	–	530	ns
			C_L = 10 pf	10	–	250	ns
f_{VCO} (Fast) to F_{VCO}/N propagation delay, falling edge to rising edge		t_{pH}	50% to 50%	5	–	250	ns
			C_L = 10 pf	10	–	175	ns
falling edge to falling edge		t_{pL}	50% to 50%	5	–	250	ns
			C_L = 10 pf	10	–	175	ns

TYPICAL DIGITAL FREQUENCY SYNTHESIZER APPLICATION





TIMING DIAGRAM OF PHASE FREQUENCY DETECTOR



NOTES: 1. ONLY POSITIVE TRANSITIONS OF f_{REF} AND f_{VCO} ARE SHOWN. CIRCUIT OPERATION IS INDEPENDENT OF DUTY CYCLES.

2. POLARITY SENSE IS TIED TO V_{DD}

APPLICATION NOTES

The Adder/Decoder, with its BCD and Binary inputs, presents a variety of application opportunities. In some cases it may be desired to input N from three BCD coded thumb wheel switches, in which case the BCD inputs are well suited. If toggle switches are used to set N, then the Binary inputs may be better suited. All unused binary and BCD inputs must be connected to a logic O (ground). In some radio transceiver applications it is desirable to offset the transmit and receive frequencies. In these applications, the channel can be set with the BCD inputs and the offset between the transmit and receive frequencies controlled with the Binary inputs (or vice-versa).

Values of 0-999/0-127 can be input on the BCD/Binary lines. However, the maximum N is 1023 and the minimum is 3.

The VCO correction output is a 3 state output which is high, low or floating. When "lock" is achieved, both the NMOS and PMOS output switches are turned off except for very narrow pulses and the output mostly "floats." An integrator and/or low pass filter is required to "smooth out" the pulses and maintain the voltage to the VCO, thus keeping the frequency constant.

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Printed in U.S.A. 1-81