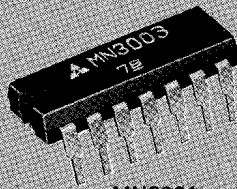
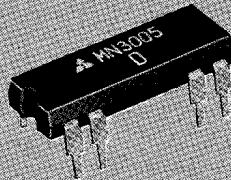


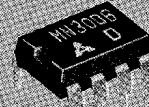
BBD's for variable delay lines in audio frequency range.



MN3001
MN3002
MN3003
MN3004
MN3010

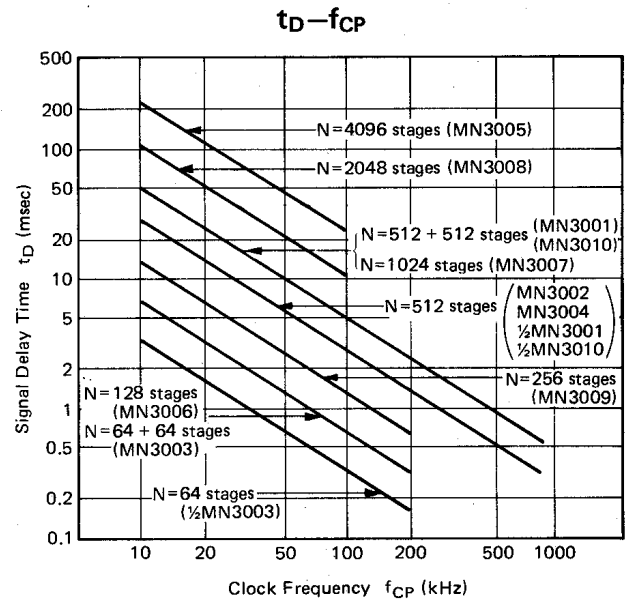


MN3005
MN3008



MN3006
MN3007
MN3009

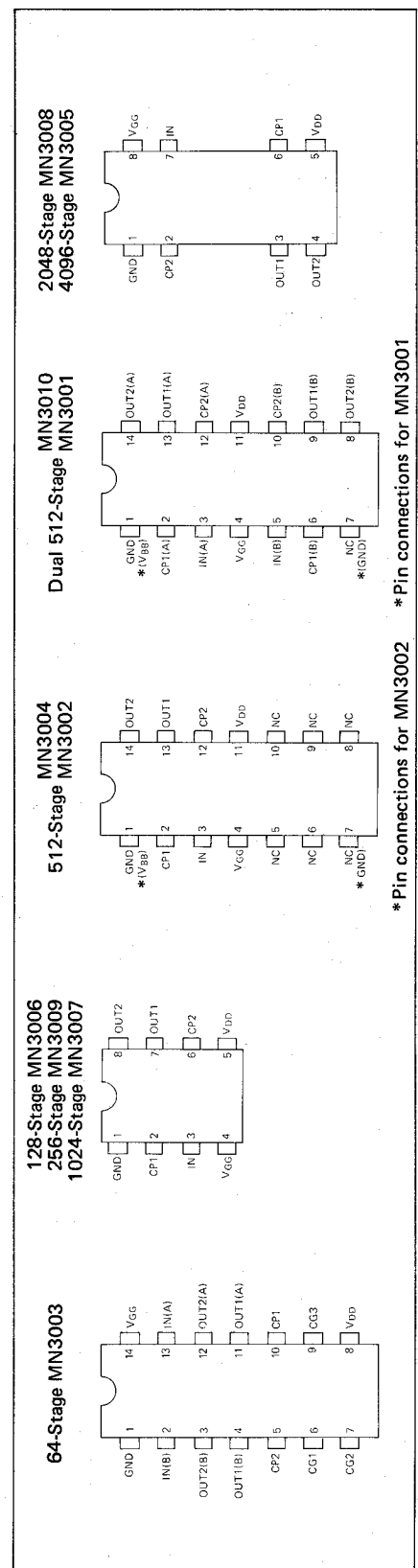
- P-channel silicon gate; tetrode MOS transistors configuration
- Signal delay: 6.4 msec to 204.8 msec
- Clock frequency range: 10 ~ 200 kHz
- Signal to noise ratio: 70dB ~ 90dB (typ.)
- Low distortion



| Stage | | Type No. | Noise | Application |
|-------|-------------|----------|-----------------|--|
| 64 | Dual Type | MN3003 | Low Noise Types | Reverberation Effect (Signal Delay under 10 msec) Vibrato Effect *1 Chorus Effect *2 Phasor/Flanger Effect *3 |
| 128 | Single Type | MN3006 | | |
| 256 | | MN3009 | | |
| 512 | Single Type | MN3004 | Standard Types | Echo Effect (Signal Delay over 10 msec.) Double Voicing Effect *4 |
| | | MN3002 | | |
| | Dual Type | MN3001 | | |
| 1024 | Single Type | MN3007 | Low Noise Types | Reverberation Effect (Signal Delay over 100 msec.) |
| 2048 | | MN3008 | | |
| 4096 | | MN3005 | | |

*1 Vibrato Effect: Several H_z modulation effect of the clock frequency for BBD.
 *2 Chorus Effect: Mixing effect of the original signal and the attenuated delayed signal.
 *3 Phasor/Flanger Effect: Effect of either the sum or difference of the original signal and the delayed signal.
 *4 Double Voicing Effect: Mixing effect of the original signal and the delayed signal.

| Item | | Symbol | MN3001 | MN3002 | MN3003 | MN3004 | MN3005 | MN3006 | MN3007 | MN3008 | MN3009 | MN3010 | Unit | |
|----------------------------|--|-------------------|-------------|------------|-----------|----------|------------------|-----------|----------|----------|------------------|-----------|-------------|------------|
| Circuit Construction | Number of BBD | | Dual-512 | 512 | Dual-64 | 512 | 4096 | 128 | 1024 | 2048 | 256 | Dual-512 | Stage | |
| | Clock Generator | | External | External | Built-in | | | | | | | | | |
| Output Terminal | Output Terminal | | External | External | Built-in | | | | | | | | | |
| | Pair | | | | | | | | | | | | | |
| Operating Conditions | Drain Supply Voltage | VDD | -15 | -15 | -9 | -15 | -15 | -15 | -15 | -15 | -15 | -15 | V | |
| | Gate Supply Voltage | VGG | -14 | -14 | -8 | -14 | -14 | -14 | -14 | -14 | -14 | -14 | V | |
| | Back-Gate Bias Voltage | VBB | +5 | | | | | | | | | | V | |
| | Clock Voltage "H" | VCPH | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | V | |
| | Clock Voltage "L" | VCPL | -15 | -15 | -9 | -15 | -15 | -15 | -15 | -15 | -15 | -15 | V | |
| Electrical Characteristics | Input DC Bias | V _{bias} | -3.3 ~ -4.9 | | -2.5 ~ -6 | -5 ~ -10 | -5 ~ -10 | -5 ~ -10 | -5 ~ -10 | -5 ~ -10 | -5 ~ -10 | -5 ~ -10 | V | |
| | Input Signal Frequency (fcp = 40kHz, 3dB down) | f _i | | 12 | | 10 | | 12 | | 12 | | 12 | kHz (max.) | |
| | Input Signal Swing | V _i | 1.8 | 0.8 | 1.8 | 1.2 | 1.8 | 1.5 | 1.5 | 1.5 | 1.7 | 1.8 | Vrms(max.) | |
| | Insertion Loss | L _i | 8.5 | 3.5 | 1.5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | dB (typ.) | |
| | Total Harmonic Distortion | THD | 0.4 | 0.5 | 0.4 | 1 | 0.2 | 0.5 | 0.5 | 0.5 | 0.3 | 0.4 | % (typ.) | |
| | Noise Level | V _N | 250 (typ.) | 100 (typ.) | 210 | 400 | 80 | 250 | 300 | 300 | 150 | 210 | μV (max.) | |
| | Signal to Noise Ratio | S/N | 70 | 75 | 85 | 75 | 90 | 80 | 78 | 88 | 88 | 85 | dB (typ.) | |
| | Signal Delay Time | t _D | 51.2 | 25.6 | 6.4 | 204.8 | 6.4 | 51.2 | 102.4 | 12.8 | 51.2 | 51.2 | msec (max.) | |
| | Package (Molded Package) | | | 14-Pin DIP | | | Larger 8-Pin DIP | 8-Pin DIP | | | Larger 8-Pin DIP | 8-Pin DIP | | 14-Pin DIP |
| | | | | 14-Pin DIP | | | Larger 8-Pin DIP | 8-Pin DIP | | | Larger 8-Pin DIP | 8-Pin DIP | | 14-Pin DIP |



The device specification are subject to change without prior notice.

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